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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,262	03/28/2001	Yasushi Miyajima	YKI-0065	1979

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EXAMINER	
WU, XIAO MIN	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,262	MIYAJIMA ET AL.	
	Examiner	Art Unit	
	XIAO M. WU	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4-11,13 and 15-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,5,15 and 16* is/are allowed.

6)☒ Claim(s) *2,6,7,13,17,18 and 20-22* is/are rejected.

7)☒ Claim(s) *8-11 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/3/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 8/3/2005 has been entered.

2. Applicant is requested to resubmit the amendment filed on 1/5/2005 since the amendment contains some character font with very poor reading.

Allowable Subject Matter

3. The indicated allowability of claims 2, 6, 7, 13, 17, 18 and 20-22 are withdrawn in view of the newly discovered reference(s) to Yanagi et al. (US Patent No. 6,359,607), Suzuki et al. (EP 0574920) and Deane (US Patent No. 5,929,489). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 7, 18 and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al. (EP 0574920).

As to claims 7, 18, Suzuki discloses an active matrix type display device (Fig. 1), comprising: a plurality of gate lines (X1-X4, Fig. 2); a plurality of data lines (Ym, Fig. 2) crossing the plurality of gate lines; a plurality of pixel electrodes (LP); a thin film transistor (Tr) disposed at each intersection between the plurality of gate lines and plurality data lines, and including a gate electrode and an active region, the gate electrode being connected to one of the plurality of gate lines, the active region having a first region connected to one of the plurality of data lines and a second region connected to a corresponding one of the plurality of pixel electrodes; and a gate line driver (1) for sequentially applying a gate selection signal with a pulse-shaped voltage waveform (Fig. (Fig. 1A) to a selected one of the plurality of gate lines; wherein the gate line driver causes a falling edge of the gate selection signal with the pulse-shaped voltage waveform to be smoother (or longer) than a rising edge thereof (see Fig. 1A), wherein, the gate line driver (1) includes a gate buffer (11) provided at a final state and connected to a corresponding one of the plurality of gate lines (X1, ...X4), the gate buffer includes a current supplying transistor (13) having first and second regions of an active layer connected between a power source and the corresponding gate line, and a current discharging transistor (12) having first and second regions of an active layer respectively connected to the ground and to the corresponding gate line, and the ratio (channel width W/ (channel length L) of the current supplying transistor differs from the ratio (channel width W)/ (channel length L) of the current discharging transistor (see col. 6, lines 30-45).

As to claims 21 and 22, Suzuki discloses that the transistor 13 is set to be greater that transistor 12 in the ration W/L (col. 6, lines 30-35).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 6, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (EP 0574920) in view of Deane (US Patent No. 5,929,489).

Note the discussion of Suzuki above. It is noted that Suzuki does not specifically disclose the transistor satisfies the condition $W/L < 1$. Deane is cited to teach a transistor for use in a LCD display device similar to Suzuki. Deane further discloses a transistor satisfies the condition $W/L < 1$ (see col. 2, lines 30-34). It would have been obvious to one of ordinary skill in the art to have modified Suzuki with the features of transistor as taught by Deane so that the effect of the parasitic transistor can be minimal (col. Lines 39).

9. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US Patent No. 6,421,038) in view of Yanagi et al. (US Patent No. 6,359,607).

As to claims 2 and 13, Lee discloses an active matrix type display device (Fig. 1), comprising: a plurality of gate lines (GL1...GLn, Fig. 1); a plurality of data lines (SL1...SLm) crossing the plurality of gate lines; a plurality of pixel electrodes (C1c); a thin film transistor (CMN) disposed at each intersection between the plurality of gate lines and plurality data lines, and including a gate electrode and an active region, the gate electrode being connected to one of the plurality of gate lines, the active region having a first region connected to one of the plurality of data lines and a second region connected to a corresponding one of the plurality of pixel electrodes; and a gate line driver (14) for sequentially applying a gate selection signal with a pulse-shaped voltage waveform (Fig. 2B) to a selected one of the plurality of gate lines; wherein the gate line driver causes a falling edge of the gate selection signal with the pulse-shaped voltage waveform to be smoother (or longer) than a rising edge thereof (see Fig. 2B, and col. 40-61). It is noted that Lee does not specifically disclose the gate selection signal requires at least a time t/2 to fall, where t is the time from when a first gate line assumes an unselected state to when subsequent second gate line assumed a selected state. Yanagi is cited to teach a LCD device similar to Lee. As shown in Fig. 1, Yanagi teaches the gate selection signal (VG(j) requires at least a time t/2 to fall (e.g. Fig. 1 shows that the time to fall is t in which satisfies at least t/2 as required), where t is the time from when a first gate line assumes an unselected state to when subsequent second gate line (VG(j+1) assumed a selected state. It would have been obvious to one of ordinary skill in the art to have modified Lee with the features of the sequentially driving the gate lines as taught by Yanagi because Yanagi is capable of sufficiently suppressing occurrence of flickering (col. 4, lines 28-32)

Allowable Subject Matter

3. Claims 4-5 and 15-16 are allowed.

10. Claims 8-11 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XIAO M. WU whose telephone number is 571-272-7761. The examiner can normally be reached on 6:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, PATRICK EDOUARD, can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

x.w.

September 2, 2005

XIAO M. WU
Primary Examiner
Art Unit 2674